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41. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a metal-comprising conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming nitride-comprising sidewall spacers directly on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

41,

after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

43. The method of claim 41, wherein the gate electrode comprises a first conductive layer a portion of which defines the interface, an overlying metal layer, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying layer.

44. The method of claim 41, wherein the forming of the sidewall spacers includes:

depositing a first material over the gate electrode;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

45. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a metal-comprising gate electrode having sidewalls and an interface with the first layer;

forming oxidation resistant sidewall spacers directly adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprised by the sidewalls; and

after forming the oxidation resistant sidewall spacers, conducting an oxidizing step by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein only a portion of the gate electrode adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized.

46. The method of claim 45, wherein the layer through which oxidants are channeled comprises a gate dielectric layer.

47. (Amended) The method of claim 45, wherein the gate structure comprises a polysilicon layer, an overlying metal layer, and an electrically conductive reaction barrier layer intermediate the polysilicon layer and the overlying metal layer.

48. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate structure;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the sidewall spacers over the gate structure's sidewalls.

49. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate structure;

anisotropically etching the first material to a degree sufficient to leave first sidewall spacers over the gate structure;

depositing a second material over the first sidewall spacers; and

anisotropically etching the second material to a degree sufficient to leave second sidewall spacers over the first sidewall spacers.

50. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a dielectric layer on a substrate;

forming a metal-comprising conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure;

44

forming a non-oxide material over the gate structure and the dielectric layer, the non-oxide material being directly against the sidewalls;

anisotropically etching the non-oxide material to form spacers on the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer; and

exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer.

51. The method of claim 50, wherein the forming of the non-oxide material and the anisotropically etching thereof comprises:

depositing a first non-oxide material over the gate structure;

anisotropically etching the first non-oxide material to a degree sufficient to leave first spacers over the gate structure sidewalls;

depositing a second non-oxide material over the first spacers; and

anisotropically etching the second non-oxide material to a degree sufficient to leave second spacers over the first spacers.

52. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

H5

covering a top and sidewalls of the gate structure with an oxidation resistant material, the sidewalls comprising a polysilicon portion, an overlying metal portion and an interposed reaction barrier portion, said covering comprising:

depositing a first barrier comprising the oxidation resistant material, the first barrier contacting the polysilicon portion, the overlying metal portion, and the interposed reaction barrier portion of the sidewalls, and

depositing a second barrier comprising the oxidation resistant material disposed over the first barrier,

anisotropically etching the oxidation resistant material to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

exposing the substrate to oxidation conditions effective to oxidize a portion of the gate structure laterally adjacent the covered sidewalls and adjacent the dielectric layer.

Please cancel claims 53-70.